UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,491	02/20/2004	Jack P. Shidemantle	650271-132	2161

45722 7590 05/14/2008

Howard IP Law Group
P.O. Box 226
Fort Washington, PA 19034

EXAMINER	
JAGAN, MIRELLYS	
ART UNIT	PAPER NUMBER
2855	
MAIL DATE	DELIVERY MODE
05/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,491	SHIDEMANTLE ET AL.	
	Examiner	Art Unit	
	Mirellys Jagan	2855	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-10,16,17,19,25,27,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10,16,17,25,27,28 and 30-34* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8-10, 16, 17, 25, 27, 28, and 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,483,190 to McGivern.

Referring to claims 8-10, McGivern discloses an interface comprising:

a logic circuit for determining a modified resistive output for a temperature sensor; and

a means for providing the modified resistive output;

wherein the means is compatible with a monitor such that the monitor can display a temperature that corresponds to the modified resistive output from the temperature probe; the means includes an FET (132) coupled to the logic circuit via a first terminal and a feedback arrangement; the means provides an FET resistance (116) corresponding to the modified resistive output; the logic circuit is programmed to execute a correlative algorithm; and the logic circuit includes a microprocessor (see figures; column 2, lines 6-9, 14-115, 29-33, 40-41; column 3, lines 30-36, 50-52; and column 5, lines 46-50).

Referring to claims 16 and 17, McGiven discloses a temperature probe comprising:

a temperature sensor having a resistive output;

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm; and

an FET for providing the modified resistive output in response to a signal from the processor;

wherein the algorithm is a predictive algorithm that converts the resistive output of the temperature sensor during a thermally unstable condition to a modified resistive output representative of a predicted temperature during a condition of thermal stability; and the processor executes an algorithm to convert the resistive output of the temperature sensor to a modified resistive output that can be displayed by a monitor.

Referring to claims 25 and 34, McGivern discloses a method for digitally modifying the resistive output of a temperature sensor, the method comprising:

inputting the resistive output from the temperature sensor to a logic circuit;

implementing a predictive or a correlative algorithm using the logic circuit to determine a modified resistive output;

controlling a gate of an FET to adopt a setting corresponding to the modified resistive output; and

outputting a resistance corresponding to the modified resistive output;

measuring an FET voltage with a first amplifier (176);

measuring a resistor voltage of a first resistor (R4) having a first resistance;

calculating an FET current using the first resistance and the resistor voltage;

calculating an FET resistance using the FET voltage and the FET current;

comparing (184) the FET resistance to the modified resistive output and applying a difference between the FET resistance and the modified resistive output as a negative feedback (200) to the gate (see figures).

Referring to claims 27 and 28, McGivern discloses a temperature probe comprising:

a temperature sensor that provides a resistive output;

a logic circuit for determining a modified resistive output for the temperature sensor; and

a means for providing the modified resistive output including an FET;

wherein the logic circuit is a microprocessor programmed to execute a predictive or a correlative algorithm; the microprocessor includes an output and the FET includes a gate; the output of the microprocessor controls the gate of the FET such that the FET provides an FET resistance corresponding to the modified resistive output; and

wherein the microprocessor further includes a first input from a first amplifier, where the first amplifier (176) measures an FET voltage of the FET; and a second input from a second amplifier, where the second amplifier (172) measures a resistor voltage of a resistor having a first resistance; wherein the microprocessor calculates an FET current using the first resistance and the resistor voltage from the second input, calculates an FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive

output and applies a difference (184) between the FET resistance and the modified resistive output as a negative feedback (200) to the gate.

Referring to claims 30 and 31, McGivern discloses an interface comprising:

a logic circuit for determining a modified resistive output for the temperature sensor; and

a means for providing the modified resistive output, wherein the means for providing the modified resistive output includes an FET;

wherein the logic circuit includes an output and the FET includes a gate, the output of the logic circuit controls the gate of the FET such that the FET provides an FET resistance corresponding to the modified resistive output; and

wherein the logic circuit further includes a second input from a second amplifier (172), where the second amplifier measures a resistor voltage of a resistor having a first resistance; the logic circuit calculates an FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

Referring to claims 32 and 33, McGivern discloses a temperature probe comprising:

a temperature sensor having a resistive output;

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm; and

an FET for providing the modified resistive output in response to a signal from the processor;

wherein the processor includes an output and the FET includes a gate, where the output of the processor controls the gate of the FET such that the FET provides an FET resistance corresponding to the modified resistive output; and

wherein the processor further includes a first input from a first amplifier, where the first amplifier measure an FET voltage of the FET, and a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance, the processor calculates an FET current using the first resistance and the resistor voltage from the second input, calculates an FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

Allowable Subject Matter

3. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not disclose or suggest the following in combination with the remaining limitations of the claims:

A temperature probe wherein the probe includes two FETs.

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mirellys Jagan whose telephone number is 571-272-2247. The examiner can normally be reached on Monday-Friday from 12PM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ed Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gail Verbitsky/

Primary Examiner, Art Unit 2855

MJ
May 7, 2008